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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,021	09/18/2003	Robert Moss	03-0172	9135

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EXAMINER	
SHIFERAW, ELENI A	
ART UNIT	PAPER NUMBER
2136	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/667,021	MOSS ET AL.	
	Examiner	Art Unit	
	Eleni A. Shiferaw	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are presented for examination.

Oath/Declaration

2. A new oath or declaration is required because the **first inventor Robert Moss has not signed the declaration**. The wording of an oath or declaration cannot be amended. If the wording is not correct or if all of the required affirmations have not been made or if it has not been properly subscribed to, a new oath or declaration is required. The new oath or declaration must properly identify the application of which it is to form a part, preferably by application number and filing date in the body of the oath or declaration. See MPEP §§ 602.01 and 602.02.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claim 7 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. It is not tangibly embodied as it is software per se. It is suggested that the claimed subject matter "A method operable within an integrated circuit to prevent unauthorized access..." should be changed to " A method operable within an integrated circuit stored in a flip-flops and registers to prevent unauthorized access...".

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Bianco et al. USPN 5,357,572.

Regarding claim 1, Bianco et al. discloses an integrated circuit (fig. 1, 3, and 6) having scan test features (col. 2 lines 29-col. 3 lines 12) and including:

a scan test signal interceptor (fig. 1 element 14, fig. 3, element 14b, and fig. 6 element 14) for intercepting scan test related signals applied to the integrated circuit (col. 4 lines 7-29, col. 4 lines 63-68, and col. 6 lines 17-39); and

a security element responsive to the scan test signal interceptor to preclude retrieval of secure information within the integrated circuit using the scan test related signals (claim 1, col. 2 lines 48-58, and col. 4 lines 7-28).

Regarding claim 7, Bianco et al. discloses a method operable within an integrated circuit (fig. 1, 3, and 6) to prevent unauthorized access to secure information (col. 2 lines 29-col. 3 lines 12), the method comprising:

detecting application of a scan test related signal to the integrated circuit (col. 4 lines 7-29, col. 4 lines 63-68, and col. 6 lines 17-39); and

precluding access to the secure information in response to detection of the scan test related signal (claim 1, col. 2 lines 48-58, and col. 4 lines 7-28).

Regarding claim 13, Bianco et al. discloses a system including an integrated circuit (fig. 1, 3, and 6) having a scan test capability (col. 2 lines 29-col. 3 lines 12), the system comprising:

means for detecting scan test operation of the integrated circuit (col. 4 lines 7-29, col. 4 lines 63-68, and col. 6 lines 17-39); and

means for precluding retrieval of secure information within the integrated circuit in response to detecting scan test operation (claim 1, col. 2 lines 48-58, and col. 4 lines 7-28).

Regarding claim 2, Bianco et al. discloses the integrated circuit wherein the security element comprises:

a reset generator to reset secure information within the integrated circuit (col. 4 lines 7-28).

Regarding claim 3, Bianco et al. discloses the integrated circuit wherein the scan test signal interceptor is operable to sense a request to enter scan test (col. 3 lines 66-col. 4 lines 28).

Regarding claim 4, Bianco et al. discloses the integrated circuit wherein the reset generator is operable to reset secure information in response the request to enter scan test (claim 1, col. 2 lines 48-58, and col. 4 lines 7-28).

Regarding claim 5, Bianco et al. discloses the integrated circuit wherein the scan test signal interceptor is operable to sense a request to exit scan test (claim 1, col. 2 lines 48-58, and col. 4 lines 7-28).

Regarding claim 6, Bianco et al. discloses the integrated circuit wherein the reset generator is operable to reset secure information in response the request to exit scan test (claim 1, col. 2 lines 48-58, and col. 4 lines 7-28).

Regarding claim 8, Bianco et al. teaches the method wherein the step of precluding includes: resetting elements of the integrated circuit to reset the secure information (col. 4 lines 7-28).

Regarding claim 9, Bianco et al. discloses the method wherein the step of detecting includes: detecting a signal applied to the integrated circuit requesting entry to scan test col. 3 lines 66-col. 4 lines 28).

Regarding claim 10, Bianco et al. discloses the method wherein the step of resetting includes: resetting elements of the integrated circuit in response to detection of the request to enter scan test (claim 1, col. 2 lines 48-58, and col. 4 lines 7-28).

Regarding claim 11, Bianco et al. discloses the method wherein the step of detecting includes: detecting a signal applied to the integrated circuit requesting exit from scan test (claim 1, and col. 2 lines 48-58).

Regarding claim 12, Bianco et al. discloses the method wherein the step of resetting includes: resetting elements of the integrated circuit in response to detection of the request to exit scan test (col. 2 lines 48-58, and col. 4 lines 7-28).

Regarding claim 14, Bianco et al. teaches the system wherein the means for precluding includes: reset means for resetting the secure information within the integrated circuit to preclude retrieval thereof using scan test operation (col. 4 lines 7-28).

Regarding claim 15, Bianco et al. discloses the system wherein the reset means is operable to generate a reset within the integrated circuit in response to sensing entry to scan test of the integrated circuit col. 3 lines 66-col. 4 lines 28).

Regarding claim 16, Bianco et al. discloses the system wherein the reset means is operable to generate a reset within the integrated circuit in response to sensing exit from scan test of the integrated circuit (claim 1, and col. 4 lines 7-28).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6990387 B1 and US 6499124 B1.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eleni A. Shiferaw whose telephone number is 571-272-3867. The examiner can normally be reached on Mon-Fri 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser R. Moazzami can be reached on (571) 272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

February 26, 2007

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2/27/07